Ultra-low jitter Differential Oscillator

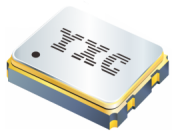
YSO233UJ

Applications

- Optical modules
- Accelerator Card

Features

- Ultra-low jitter: 0.03ps Typ.@156.25MHZ
- Output: LVPECL, HCSL or LVDS
- Package Size: 2.0*1.6,2.5*2.0, 3.2*2.5



Specifications (规格参数)

Item/Type	LVPECL	LVDS	HCSL	Remarks
	2016/2520/3225			
Output Frequency 额定频率	100, 125, 156.25, 200, 212.5, 312.5MHZ			For special requirements, please contact us.
Supply Voltage 电源电压	2.5V ,3.3V	1.8V,2.5V ,3.3V	1.8V,2.5V ,3.3V	
Operating Temperature Range 工作温度	-40~+105°C, or specify			
Storage Temperature Range 储存温度	-55~+125°C			
Total Stability 频率偏差	±20ppm, ±50ppm, or specify			Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature
Current Consumption 消耗电流	65mA Max			OE=VDD, LVPECL=(50)Ω, HCSL=(50)Ω or LVDS=(100)Ω
Standby Current 待机电流	60uA Max			OE=GND
Differential Output Swing 差分输出摆幅	1000mV Max	450mV Max	950mV Max	
Output Voltage (LVPECL) 输出电压 (LVPECL)	VOH=VDD-1.1V Min	--	--	DC characteristics
	VOL=VDD-1.5V Max	--	--	
Output Voltage (LVDS) 输出电压 (LVDS)	--	VOH=1.6V Max	--	DC characteristics
	--	VOL=0.9V Min	--	
Output Voltage (HCSL) 输出电压 (HCSL)	--	--	VOH= 1.0V Max	DC characteristics
	--	--	VOL= -0.15V Min	
Output Load Condition 输出负载	L_PECL=50Ω	--	--	Terminated to VDD-2.0V
	--	L_LVDS=100Ω	--	Connected between OUT to OUT
	--	--	L_HCSL=50Ω	--
Input Voltage 输入电压	VIH=80% VDD Min, VIL=20%VDD Max			OE terminal
Duty Cycle 占空比	45~55%			
Rise Time/Fall Time 上升沿/下降沿	0.4nS Max			LVPECL: Between 20% and 80% of (VOH-VOL), LVDS: Between 20% and 80% Differential Output peak to peak voltage
Start-up time 启动时间	10mS			Time at minimum supply voltage to be 0 s
Aging 老化率	±3ppm			25°C First year
RMS Jitter [12 kHz ~ 20 MHz] 相位抖动	50fs Typ.@100MHZ			
	40fs Typ.@156.25MHZ			
	30fs Typ.@312.5MHZ			

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Phase Noise（相位噪声）

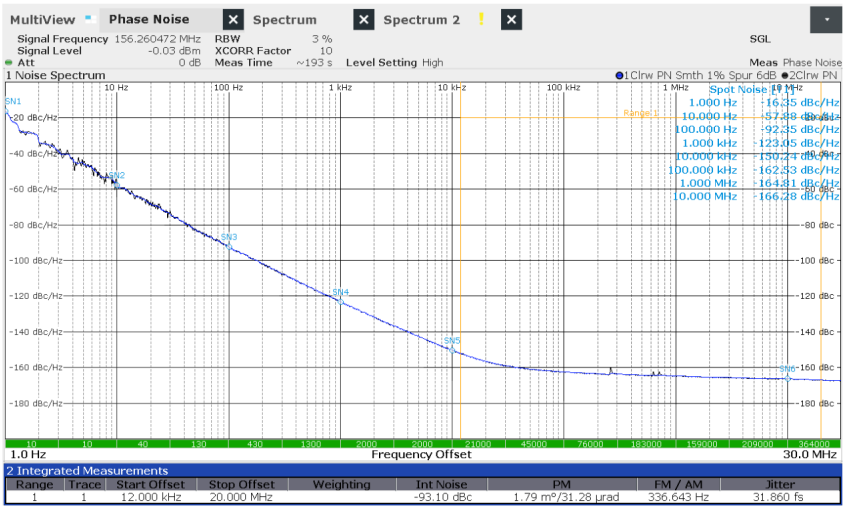

Figure 1.LVDS output phase noise plot@156.25M

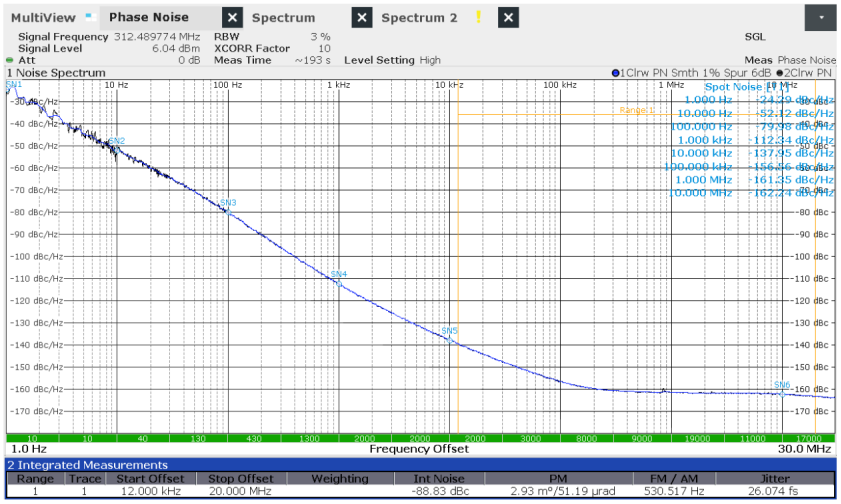

Figure 2.LVPECL output phase noise plot@312.5M

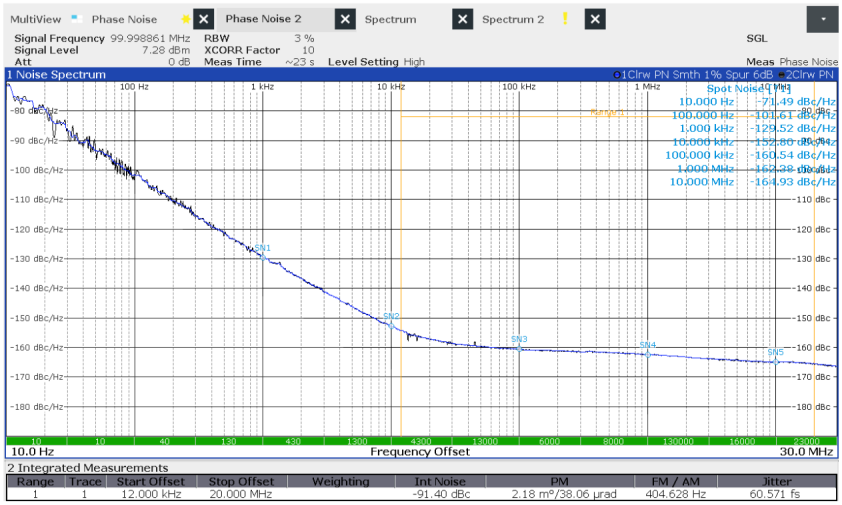

Figure 3.HCSL output phase noise plot@100M

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Pin Dimension (脚位尺寸)

Pin	#1	#2	#3	#4	#5	#6
FUNCTION	OE	NC	GND	OUT+	OUT-	VDD

Notes: To maintain stable operation provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between VDD-GND).

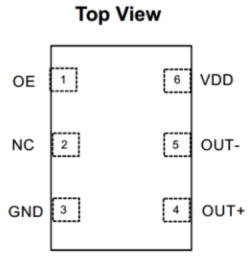
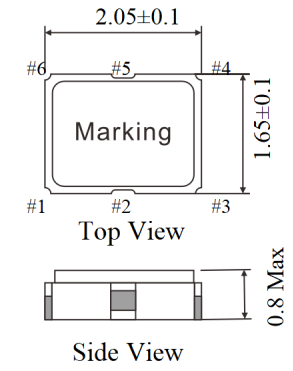
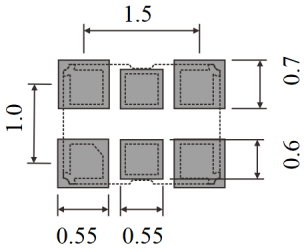
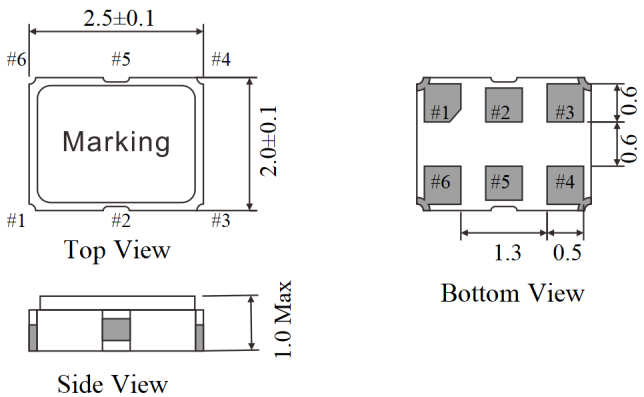
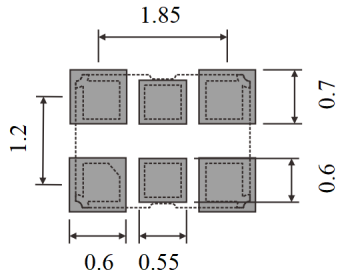


Figure 4.Pin Assignments

Dimensions and Recommended Land Pattern (外观尺寸及推荐焊盘)

Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
2.0*1.6mm  	 Recommended soldering Pattern
2.5*2.0mm  	 Recommended soldering Pattern

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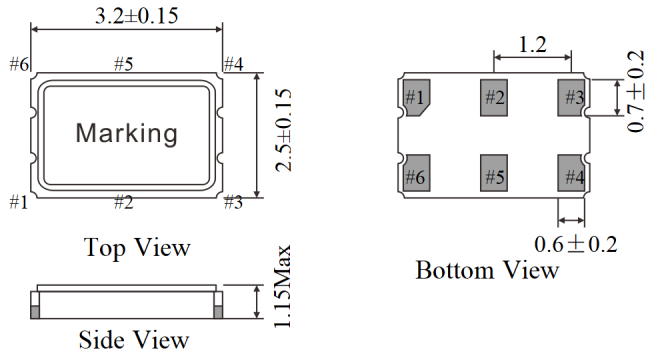
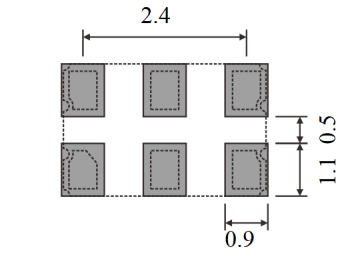
3.2*2.5mm

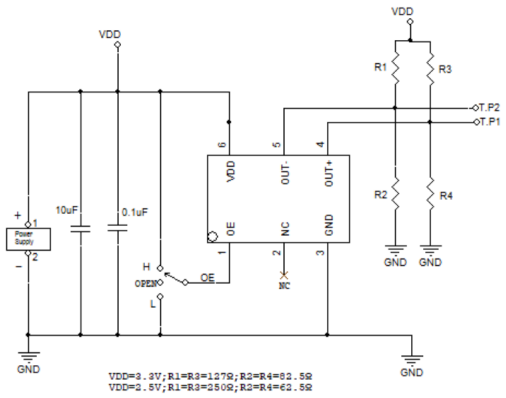
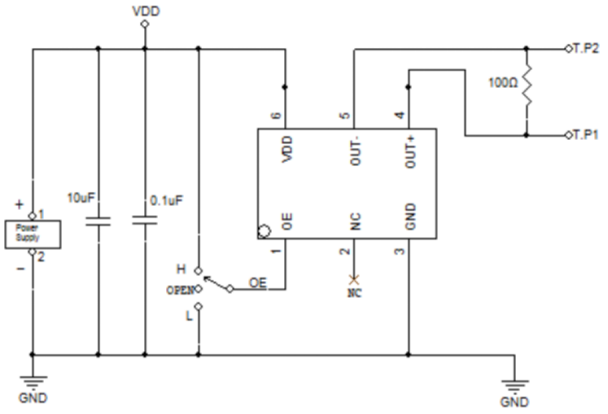




Recommended soldering Pattern

Notes:
1.A capacitor of value 0.01uf~0.1uf or higher between VDD and GND is required.

Test Circuit (测试电路)

LVPECL	LVDS
	
HCSL	**LVDS Test Circuits for 1.8V only**