

Temperature Compensated Crystal Oscillator YSO510TP TCXO



Applications

- Networking
- Industrial

Features

- Frequency Stability as Tight as ± 1.0 ppm Over -40°C to 85°C
- Package Size : 2.0*1.6, 2.5*2.0, 3.2*2.5, 5.0*3.2, 7.0*5.0mm
- Ultra Small SMD Seam Sealed Crystal Oscillator



Specifications (规格参数)

Item/Type	Clipped Sine Wave or CMOS				
Package Size 封装尺寸	2.0 x 1.6	2.5 x 2.0	3.2 x 2.5	5.0 x 3.2	7.0 x 5.0
Frequency Range 额定频率范围	26 ~ 52MHz	13 ~ 52MHz	13 ~ 52MHz	6.4 ~ 52MHz	6.4 ~ 52MHz
Supply Voltage 电源电压	1.8V, 2.5V, 3V, 3.3V				
Operating Temperature Range 工作温度	-30 ~ +85°C, or specify				
Storage Temperature Range 储存温度	-40°C to +85°C				
Output Type 输出方式	Clipped Sine wave or CMOS				
Current Consumption (max.) 消耗电流	Clipped Sine Wave: 3.5mA (Max) CMOS: 1.8V/2.5V:10mA (Max); 3V/3.3V:13mA (Max)				
Duty Cycle 占空比	40~60%				
Output Voltage Level (peak to peak) 峰峰值	Clipped Sine Wave: 0.8 Vp-p Min. CMOS: VOH = 80%Vdd(Min.) / VOL = 20%Vdd(Max.)				
Start-up Time 启动时间	2.0msec (Typ.), 5.0msec (Max.) @ +25 ± 2°C				
Initial Calibration Tolerance 初始校准公差	± 2.0 ppm (Max.) at +25°C $\pm 2^\circ$ C (at the shipment)				
Output Load 输出负载	Clipped Sine Wave: 10K Ω // 10pF $\pm 10\%$ CMOS: 15pF				
Frequency Stability 频率偏差	vs Aging at Ta = +25°C	± 1.0 ppm / year (Max.)			
	vs Voltage Change	± 0.2 ppm (Max.), for a $\pm 5\%$ input voltage change			
	vs Load Change	± 0.2 ppm (Max.), for a $\pm 10\%$ load condition change			
	vs Reflow	± 2.5 ppm (Max.)			
	vs Temperature Change	5ppm / ± 2.5 ppm			
Phase Noise@10MHZ 相位噪声	-150dBc / Hz @ 1KHz (Min.)				

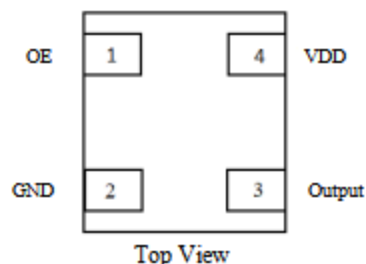
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Pin Description-CMOS (脚位说明-CMOS)

Pin	#1	#2	#3	#4
Function	Output Enable	Ground	Output	Supply Voltage

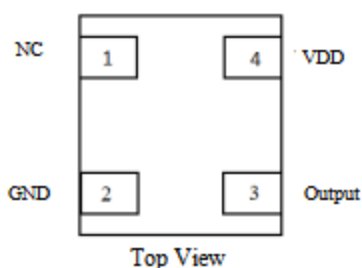
Pin Assignments-CMOS



Pin Description-Clipped sine wave (脚位说明-Clipped sine wave)

Pin	#1	#2	#3	#4
Function	No Connect	Ground	Output	Supply Voltage

Pin Assignments-Clipped sine wave



Notes:

1. Please keep the NC pin floating during use. Do not connect it to any network (power, ground, or signal).
2. The provided pinout is for reference purposes only. The definitive material specification document must be obtained by contacting a sales representative.

Dimensions and Recommended Land Pattern (外观尺寸及推荐焊盘)

Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
<p>2.0*1.6mm</p> <p>Top View: Overall width 2.05±0.15, height 1.65±0.15. Pin 1 is on the left, pin 4 on the right. Marking is in the center.</p> <p>Bottom View: Pin 1 and 2 on the top, pin 4 and 3 on the bottom. Pin 1 width 0.4, pin 2 width 0.625. Pin 4 width 0.4, pin 3 width 0.625. Pin 1-4 distance 1.2±0.1.</p> <p>Side View: Maximum height 0.8mm.</p>	<p>Recommended soldering Pattern: Pad width 0.6, pad height 0.8, pad spacing 1.1±0.1, and pad offset 0.4.</p>

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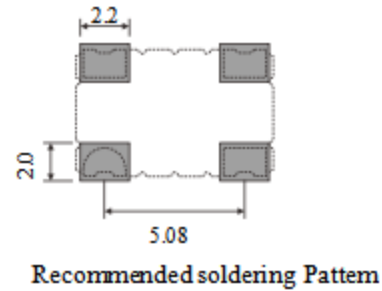
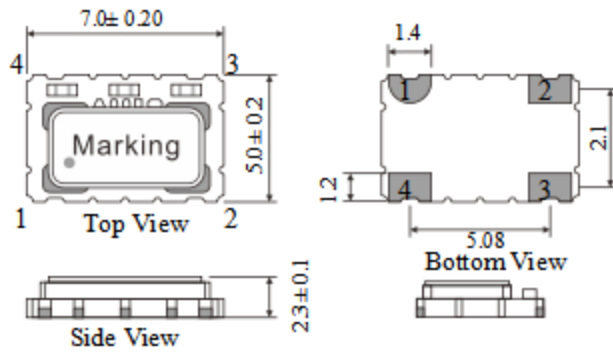


<p>2.5*2.0mm</p> <p>Top View</p> <p>Bottom View</p> <p>Side View</p>	<p>Recommended soldering Pattern</p>
<p>3.2*2.5mm</p> <p>Top View</p> <p>Bottom View</p> <p>Side View</p>	<p>Recommended soldering Pattern</p>
<p>5.0*3.2mm</p> <p>Top View</p> <p>Bottom View</p> <p>Side View</p>	<p>Recommended soldering Pattern</p>

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7.0*5.0mm

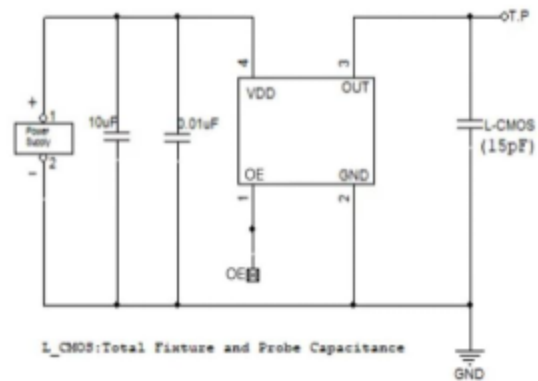
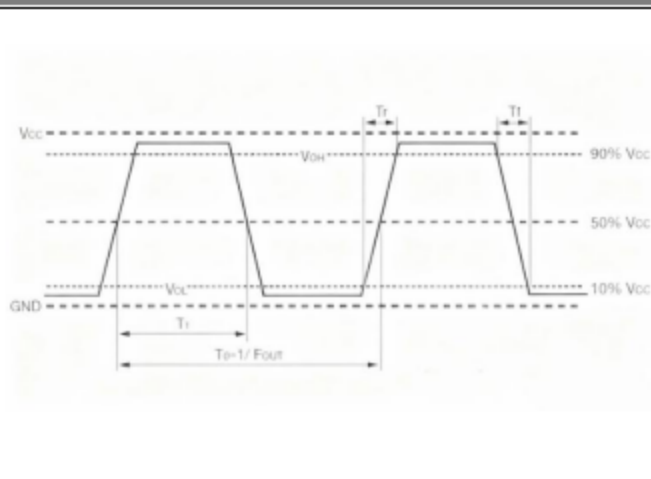


Notes:

1. A capacitor of value 0.01 μ F-0.1 μ F or higher between Vdd and GND is required.
2. The package outlines are for reference purposes only. The definitive material specification document must be obtained by contacting a sales representative.

Output Waveform and Test Circuit (输出波形和测试电路)

CMOS



Clipped Sine Wave

