

# Crystal Oscillator

## YSO212PU

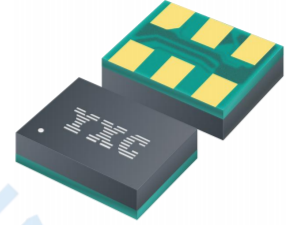


### General Description (概述)

**YSO212PU is a programmable, low-jitter differential crystal oscillator.** Output frequency is factory programmed as per customer requirements between **200 kHz to 1.5 GHz**. YSO212PU is a low Noise PLL with Integrated XTAL which provides clocks with Jitter of **69 fs**.

With on chip NVM and factory programming, we can service customer

requirements with very fast lead times.



### Features (产品特性)

- Available with any frequency from 200 kHz to 1.5 GHz
- Low Jitter: 69fs@156.25MHz Typ Jrms, 12 kHz – 20 MHz
- 26fs Typ Jrms, 12 kHz – 20 MHz with 4 MHz HPF
- Fractional N fully integrated PLL
- 3.3 V, 2.5 V and 1.8 V VDD supply operation
- Best in class PSRR performance of -85 dBC
- LVPECL, HCSL-LP, LVDS, LVDS-Boost, HCSL, AC Coupled CML output options available on differential output pads.
- HCSL-LP Output Driver type frequency support is from 20 kHz to 500MHz
- $\pm 50$  ppm stability (-40°C to 85 °C)
- Package Options: Available in 6pin Plastic Package : 3.2\*2.5mm, 2.5\*2.0mm, 2.0\*1.6mm

### Applications (应用领域)

- 100G/200G/400G OTN, coherent optics
- 10G/40G/100G optical ethernet
- 3G-SDI/12G-SDI/24G-SDI broadcast video
- Datacenter
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clocking

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### 1 Specifications (规格参数)

Table 1 Electrical Characteristic

Item/Type	Min	Typ	Max	Remarks
Output Frequency Range 额定频率范围	200K~1.5GHz			
Supply Voltage 电源电压	1.71V	1.8V	1.89V	Voltage Tolerance: $\pm 5\%$
	2.375V	2.5V	2.625V	
	3.135V	3.3V	3.465V	
Current Consumption 消耗电流	LVPECL	71mA		F <sub>out</sub> =156.25M
	LVDS	53mA		
	LVDS-Boost	57mA		
	HCSL	66mA		
	HCSL-LP	50mA		
Input Voltage 输入电压	V <sub>IH</sub> =70% VDD Min V <sub>IL</sub> =30%VDD Max			OE terminal
Output Disable Time 输出禁用时间		1 us + 3clock Cycles us	2 us + 3clock Cycles us	F <sub>CLK</sub> > 10 MHz
Output Enable Time 输出启用时间		1 us + 3clock Cycles us	2 us + 3clock Cycles us	
Operating Temperature Range 工作温度	-40~+85°C, or specify			
Total Stability 频率偏差	$\pm 50$ ppm, or specify			Total stability includes frequency tolerance(initial accuracy),temperature stability,load and VDD variation and 10 year aging at 25°C
Start-up time 启动时间	10mS			

Table 2 Absolute Maximum Ratings

Item/Type	Min	Typ	Max	Remarks
Core Supply Voltage 核心工作电压	-0.5V		3.63V	
Voltage range (All inputs) 输入引脚电压范围	-0.5V		3.63V	Relative to GND
Maximum Junction Temperature in Operation 最大工作温度			+125°C	
Storage Temperature Range 储存温度	-55°C		+150°C	
Programming Voltage 编程电压	2.375V	2.5V	2.625V	
Latch Up 闩锁效应	100 mA Max			
ESD 静电防护	Human body model: 2000V Max			
	Charged device model: 500V Max			

Notes:

- Exceeding maximum ratings may shorten the useful life of the device.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

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Table 3 Output Clock Specifications

Parameter		Symbol	Min	Typ	Max	Units
<b>LVDS Outputs</b>						
Output Common-Mode Voltage 输出共模电压	VDD=2.5/3.3V	Vocm	1.125	1.25	1.375	V
	VDD=1.8V		0.75	0.85	1.0	
Clock Output Frequency 时钟输出频率		Fout	0.2		1500	MHz
Output Rise/Fall Time 上升下降时间		Trf			350	ps
Output differential peak 输出差分峰值	@156.25M	VP		400		mV
	≤700M		250		500	
	>700M/<1500M		250		500	
<b>LVDS-Boost Outputs</b>						
Clock Output Frequency 时钟输出频率		Fout	0.2		1500	MHz
Output Rise/Fall Time 上升下降时间		Trf			350	ps
Output differential peak 输出差分峰值	@156.25M	VP		800		mV
	≤700M		600		950	
	>700M/<1500M		500		950	
<b>LVPECL Outputs</b>						
Output High Voltage 输出高电压	VDD=2.5/3.3V	VOH	VDD-1.165		VDD-0.8	V
Output Low Voltage 输出低电压		VOL	VDD-2		VDD-1.55	
Clock Output Frequency 时钟输出频率		Fout	0.2		1500	MHz
Output Rise/Fall Time 上升下降时间		Trf			350	ps
Output differential peak 输出差分峰值	@156.25M	VP		720		mV
	≤700M		500		1050	
	>700M/<1500M		400		800	
<b>HCSL Outputs</b>						
Output High Voltage 输出高电压	VDD=1.8/2.5/3.3V	VOH	0.65	0.83	1.05	V
Output Low Voltage 输出低电压		VOL	-0.1	0	0.1	
Clock Output Frequency 时钟输出频率		Fout	0.2		1500	MHz
Output Rise/Fall Time 上升下降时间		Trf			350	ps
Far End Termination Output differential peak 输出差分峰值	@156.25M	VP		800		mV
	≤700M		400		1050	

Table 3 (Continued)

HCSL-LP Outputs						
Output High Voltage 输出高电压	VDD=1.8/2.5/3.3V	VOH	0.7	0.8	0.9	V
Output Low Voltage 输出低电压		VOL	-0.1	0	0.1	
Clock Output Frequency 时钟输出频率		Fout	0.2		500	MHz
Output Rise/Fall Time 上升下降时间		Trf			350	ps
Output differential peak 输出差分峰值	@156.25M	VP		720		mV
	≤500M		500		900	

### 1.1 Phase Jitter (相噪抖动)

Table 4 Output RMS Jitter and Phase Noise

Item/Type	Value	Remarks
RMS Jitter [ 12 kHz ~ 20 MHz ]	69fs rms Typ.	@156.25MHz
RMS Jitter for [ 12 kHz ~ 20 MHz ]Integration Bandwidth with 4MHz High Pass Filter	26fs rms Typ.	
Phase Noise	-35 dBc/Hz@1Hz	
	-73 dBc/Hz@10Hz	
	-102 dBc/Hz@100Hz	
	-126 dBc/Hz@1kHz	
	-137 dBc/Hz@10kHz	
	-146 dBc/Hz@100kHz	
	-150 dBc/Hz@1MHz	
-161 dBc/Hz@10MHz		

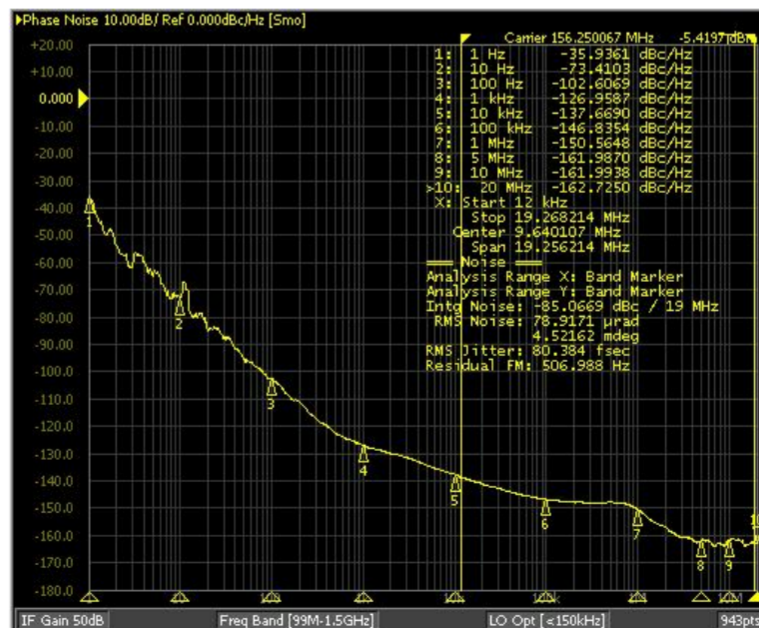


Figure 1 Representative Phase Noise Measurement@156.25M

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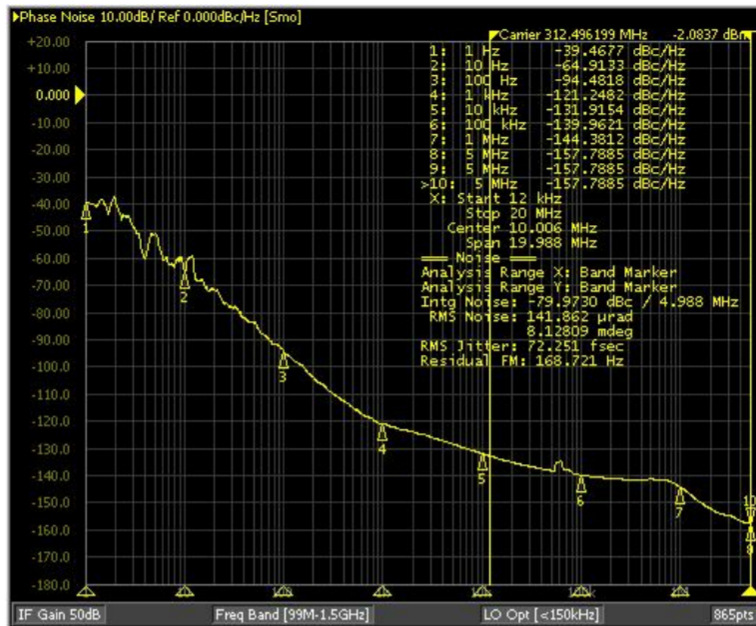


Figure 2 Representative Phase Noise Measurement@312.5M

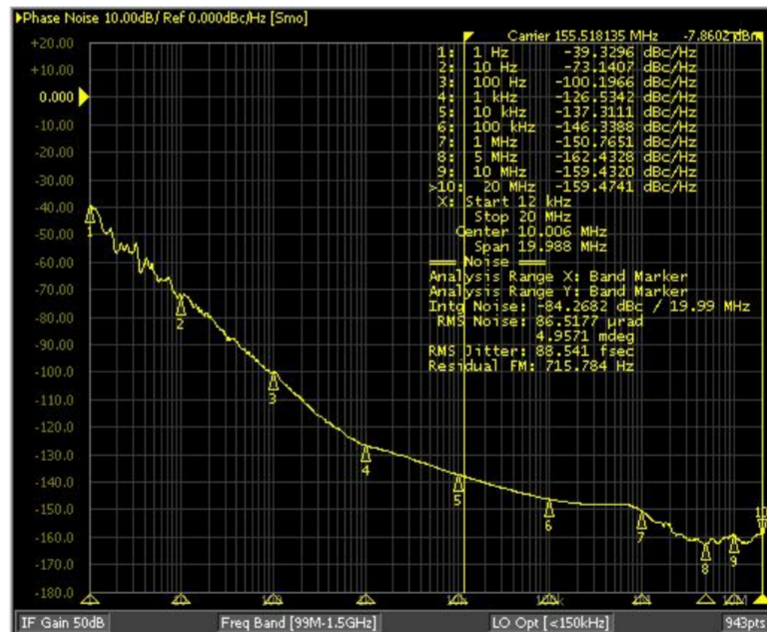


Figure 3 Representative Phase Noise Measurement@155.52M

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## 1.2 Frequency vs Temperature Test (频率-温度特性测试)

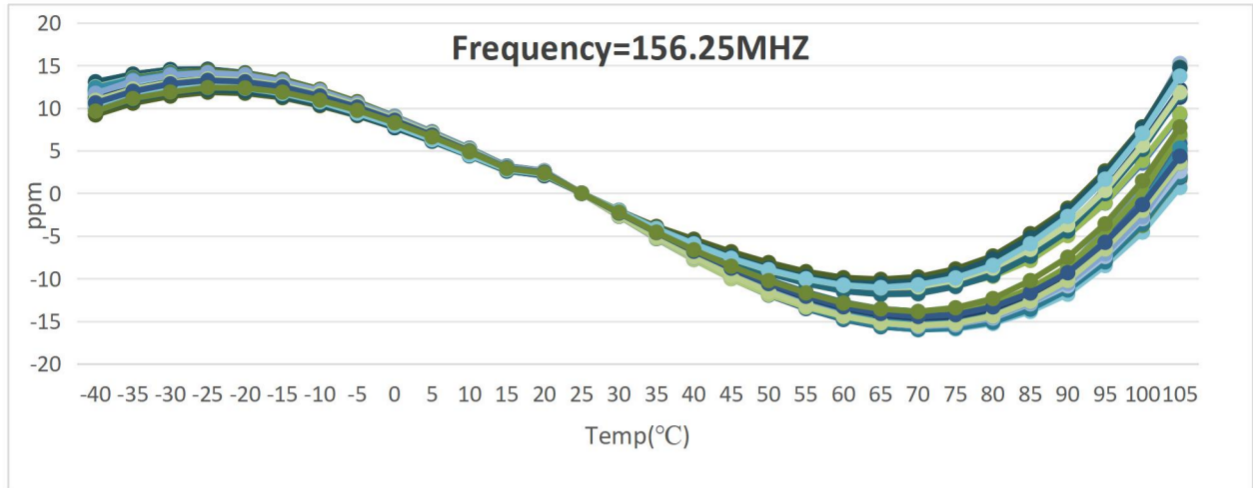


Figure 4 Frequency vsTemperature

## 2 Pin Dimension (脚位尺寸)

Table 5 Pin Description

Pin Name	Pin No.	I/O Type	Description
OE/NC	1,2	Input	Selectable by Ordering Information OE = Output Enable ; NC = No connect
GND	3		GND
CLKP	4	Output	Clock + for differential Output.
CLKN	5	Output	Clock - for differential Output.
VDD	6	Power	Chip Power Supply

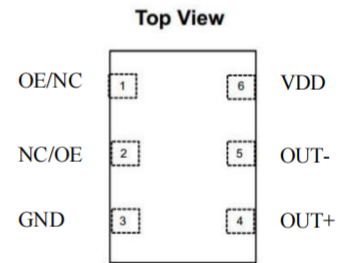


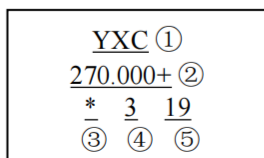
Figure 5 Pin Assignments

Notes: The Output Enable Pin can be configured as Active High or Low based on the customer requirement.

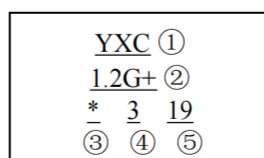
### 3 Dimensions and Recommended Land Pattern (外观尺寸及推荐焊盘)

Dimensions (Unit: mm)		Recommended Land Pattern (Unit: mm)
<p>2.0*1.6mm</p> <p>Top View</p> <p>Side View</p> <p>Bottom View</p>	<p>Recommended soldering Pattern</p>	
<p>2.5*2.0mm</p> <p>Top View</p> <p>Side View</p> <p>Bottom View</p>	<p>Recommended soldering Pattern</p>	
<p>3.2*2.5mm</p> <p>Top View</p> <p>Side View</p> <p>Bottom View</p>	<p>Recommended soldering Pattern</p>	

### 4 Marking information (丝印说明)



or



① YangXing LOGO
② Frequency
③ Line
④ Year
⑤ Production Cycle

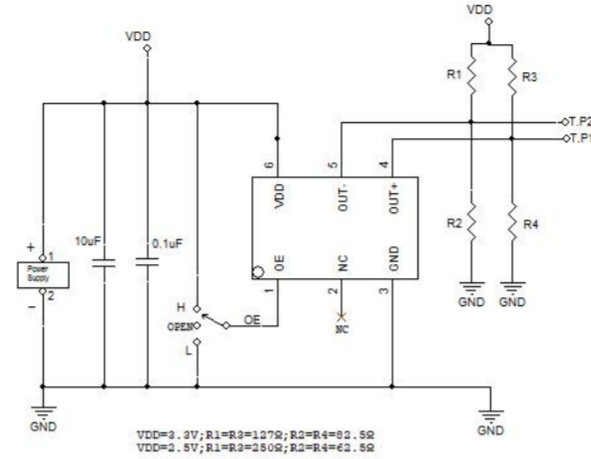
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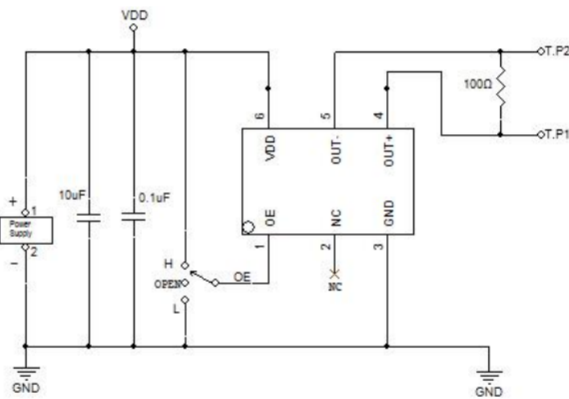
### 5 Test Circuit (测试电路)



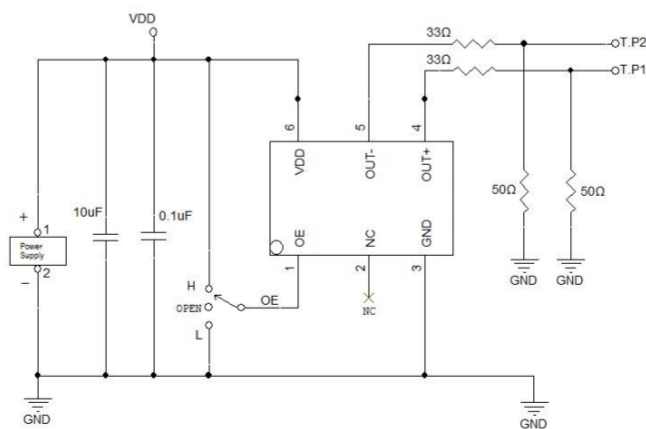
#### LVPECL



#### LVDS/LVDS-Boost



#### HCSL/HCSL-LP



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### 6 Reflow profile (回流焊)

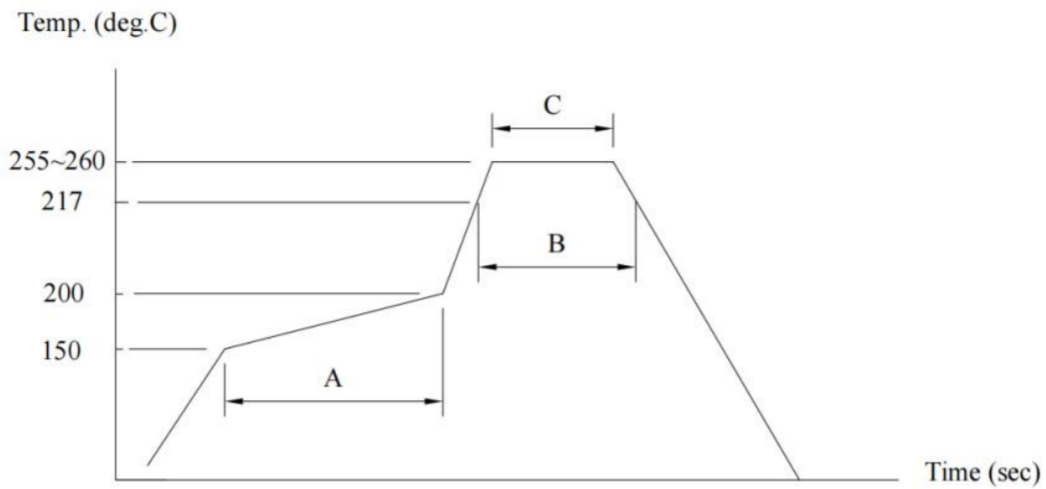
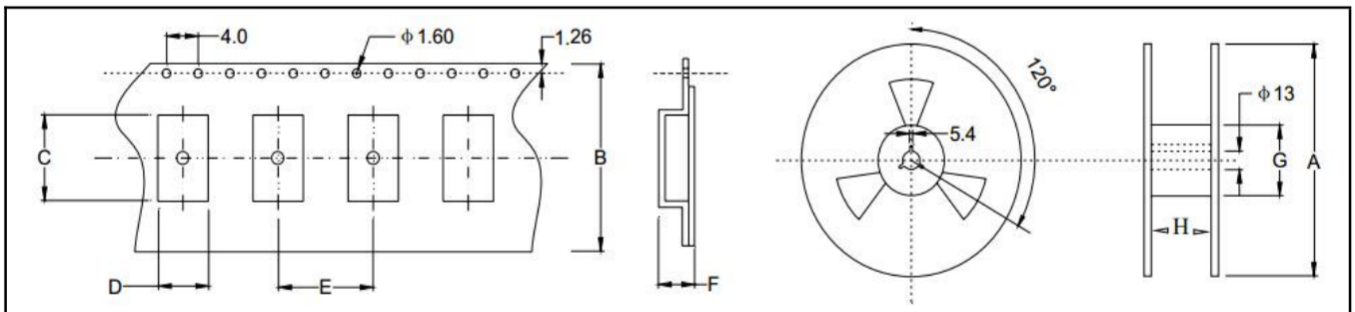


Figure 6. Reflow Profile

- (A)→Preheating area : 150~200°C, 60~120sec.
- (B)→Heating area : 217°C, 60~150sec.
- (C)→Peak temperature : 255~260°C, 30sec. Max.
- Ramp-up rate (217→260°C) : 3°C/sec. Max.
- Ramp-down rate (260→217°C) : 6°C/sec. Max.
- Time 25°C→260°C : 480sec. Max.

### 7 Taping Specification (载带规格) (Unit: mm)



Size	A	B	C	D	E	F	G	H	Pcs/reel
SMD-2016	180±2.0	8.0±0.3	2.30±0.1	1.90±0.1	4.0±0.1	0.65±0.1	61.0±1.0	9.5±0.5	3000
SMD-2520	180±2.0	8.0±0.3	2.70±0.1	2.25±0.1	4.0±0.1	0.8±0.1	61.0±1.0	9.5±0.5	3000
SMD-3225	180±2.0	8.0±0.3	3.40±0.1	2.70±0.1	4.0±0.1	1.40±0.1	61.0±1.0	9.5±0.5	3000

