

Differential Oscillator

YSO231LJ



Applications

– 10 GB Ethernet,
SONET, SATA, SAS,
Fibre Channel

Features

– Femto second integrated phase jitter (50 fs typical , 12 KHz to 20 MHz)
– Output LVPECL, LVDS or HCSL.
– Superior phase noise (-157 dBc/Hz at 100 KHz and -164 dBc/Hz at 10 MHz offset)

– Package Size: 2.5*2.0 , 3.2*2.5 , 5.0*3.2
7.0*5.0mm.



Specifications

Item/Type	LVPECL	LVDS	HCSL				
Output Frequency Range	100~250MHZ	100~250MHZ	100~175MHZ				
Supply Voltage	2.5V, 3.3V	1.8V, 2.5V, 3.3V	1.8V, 2.5V, 3.3V				
Operating Temperature Range	-40~+85℃,or specify						
Storage Temperature Range	-55~+150℃						
Total Stability	±25ppm, ±50ppm, ±100ppm or specify						
Current Consumption	52mA(Typ) 65mA(Max)	22mA(Typ) 30mA(Max)	32mA(Typ) 40mA(Max)				
Output Swing (single-end)	400 mV (min.)	200 mV (min.)	450 mV (min.)				
Output Load Condition	50 Ω into VDD - 2.0V or Thevenin equivalent	100 Ω between output and complimentary output	50 Ω to ground on each output				
Duty Cycle	45~55%						
Rise Time/Fall Time(20%↔80% of waveform)	0.15ns(Typ) 0.4ns(Max)	0.15ns(Typ) 0.3ns(Max)	0.2ns(Typ) 0.6ns(Max)				
Start-up time	1ms(Typ) 5ms(Max)						
Aging	±3ppm(Max)						
RMS Jitter (12 KHz to 20 MHz)	50 fsec (typ.) , 300 fsec (max.) [For 125 MHz , LVDS , 3.3V]						
Phase Noise[dBc / Hz (typ.)]	Offset	100Hz	1KHz	10KHz	100KHz	1MHz	10MHz
	125.0MHz	-114	-135	-147	-157	-163	-164
	156.250MHz	-108	-132	-141	-152	-160	-161

Dimensions and Patterns [unit:mm]

Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
2.5*2.0mm Top View Bottom View Side View Pad Connections : Pad 1 : OE Pad 4 : Output Pad 2 : No Connection Pad 5 : Complementary Pad 3 : Ground Pad 6 : Supply Voltage	Land Pattern Top View Suggested Layout

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3.2*2.5mm Top View: 3.2 ± 0.1, 2.5 ± 0.1, Marking Bottom View: 0.6, 0.8, 1.2, 1, 2, 3, 4, 5, 6 Side View: 1.0 ± 0.1 Pad Connections: - Pad 1: OE - Pad 2: No Connection - Pad 3: Ground - Pad 4: Output - Pad 5: Complementary - Pad 6: Supply Voltage	Land Pattern Top View Suggested Layout
5.0*3.2mm Top View: 5.0 ± 0.2, 3.2 ± 0.2, Marking Bottom View: 0.1, 2.54, 2.1, 0.9, 0.64, 1, 2, 3, 4, 5, 6 Side View: 1.2 ± 0.1 Pad Connections: - Pad 1: OE - Pad 2: No Connection - Pad 3: Ground - Pad 4: Output - Pad 5: Complementary - Pad 6: Supply Voltage	Land Pattern Top View Suggested Layout
7.0*5.0mm Top View: 7.0 ± 0.2, 5.0 ± 0.2, Marking Bottom View: 1.4 ± 0.1, 5.08, 3.7, 1.2 ± 0.1, 1, 2, 3, 4, 5, 6 Side View: 1.7 ± 0.1 Pad Connections: - Pad 1: OE - Pad 2: No Connection - Pad 3: Ground - Pad 4: Output - Pad 5: Complementary - Pad 6: Supply Voltage	Land pattern Top View Suggested Layout

Test Circuit

LVDS	LVPECL	HCSL
$V_{DD} = 3.3V$; $R1 = R3 = 127\ \Omega$; $R2 = R4 = 82.5\ \Omega$ $V_{DD} = 2.5V$; $R1 = R3 = 250\ \Omega$; $R2 = R4 = 62.5\ \Omega$		$R_s = 0$ to $33\ \Omega$ to minimize ringing in application.