

PROGRAMMABLE CRYSTAL OSCILLATOR

YSV220PR VCXO



Applications

10 GB Ethernet,
SONET, SATA, SAS,
Fibre Channel

Features

Freq range:10MHz-1500MHz.
Output LVPECL or LVDS.

Package Size: 3.2*2.5 , 5.0*3.2 7.0*5.0mm.
High precision characteristic covering up
to wide frequency range.



Specifications

Item/Type	SMD VCXO	LVPECL	LVDS	Remarks	
Output Frequency Range		10MHZ~1500MHZ			
Supply Voltage		2.5Vdc ± 10% 3.3Vdc ± 10%			
Operating Temperature Range		-40~+85℃,or specify			
Storage Temperature Range		-55~+125℃			
Total Stability		±50ppm			
Absolute Pull Range		±50ppm Min,			
Input Resistance		1Mohms Typ			
Current Consumption		80mA Max	50mA Max	OE=Vcc, LVPECL=(50)Ω or LVDS=(100)Ω	
Disable Current		16mA Typ		OE=GND	
Output Voltage (LVPECL)		VOH=Vcc-1.03 Min	--	DC characteristics	
		VOL=Vcc-1.6 Max	--		
Output Voltage (LVDS)		--	VOD= 175mV	VOD1, VOD2	DC characteristics
		--	dVOD=50mV Max.	dVOD= VOD1-VOD2	
		--	VOS= 1.25V	VOS1, VOS2	
		--	dVOS=50mV Max.	dVOS= VOD1-VOD2	
Output Load Condition		L_PECL=50Ω	--	Terminated to Vcc-2.0V	
		--	L_LVDS=100Ω	Connected between OUT to OUT	
Input Voltage		VIH=70% VccMin, VIL=30%Vcc Max		OE terminal	
Output Symmetry		45~55%			
Rise Time/Fall Time		1nS Max		LVPECL: Between 20% and 80% of (VOH-VOL), LVDS:Between 20% and 80% Differential Output peak to peak voltage	
Start-up time		10mS		Time at minimum supply voltage to be 0 s	
Aging		±3ppm		25℃First year, Vcc=2.5V,3.3V	
Phase Jitter(12KHZ~20MHZ)		1.0ps Typ.		200MHZ~800MHZ	
		2.0ps Typ.		801MHZ~1500MHZ	

Pin Dimension

Pin	#1	#2	#3	#4	#5	#6
FUNCTION	Vcon	OE	GND	OUT+	OUT-	VDD

Notes: To maintain stable operation provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc-GND).

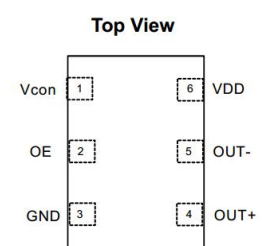


Figure 1. Pin Assignments

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Dimensions and Patterns [unit:mm]



Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
3.2*2.5mm Top View Bottom View Side View	Top View Suggested Layout
5.0*3.2mm Top View Bottom View Side View	Top View Suggested Layout
7.0*5.0mm Top View Bottom View Side View	Top View Suggested Layout
Notes: 1.A capacitor of value 0.01uf~0.1uf or higher between Vdd and GND is required.	

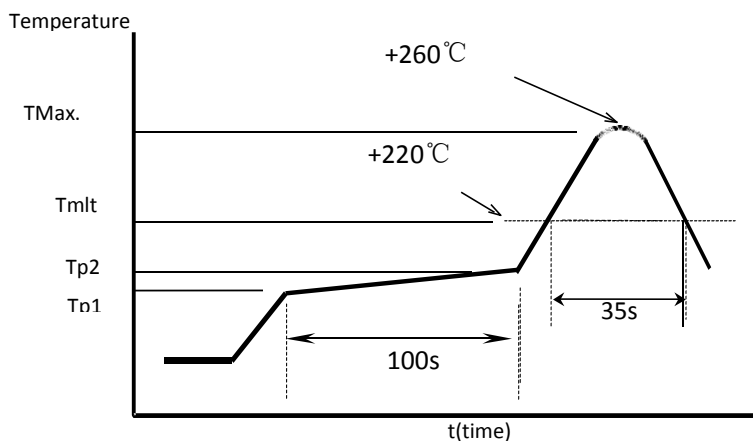
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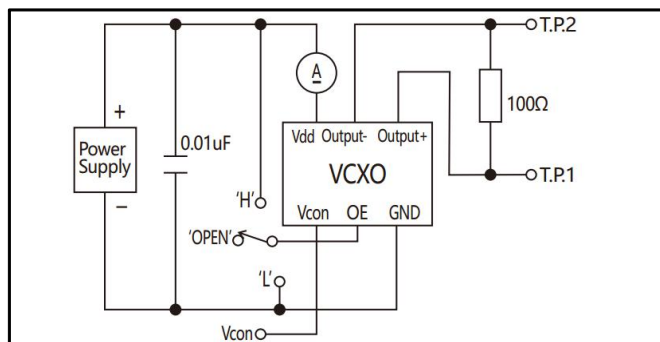
Reflow Soldering Profile

Pre Heating Temperature $T_{p1} \sim T_{p2} = +170\text{ }^{\circ}\text{C}$
 Heating Temperature
 $T_{Mlt} = +220\text{ }^{\circ}\text{C}$
 Peak Temperature
 $T_{Max.} = +260\text{ }^{\circ}\text{C}$
 Point of measuring
 In case of Solder ability Terminal.
 In case of Resistance to soldering heat Surface.

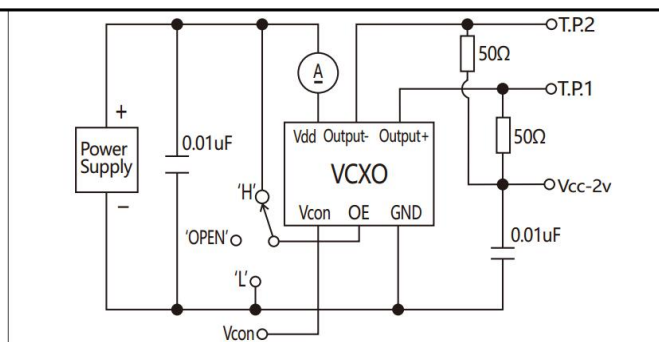


Test Circuit

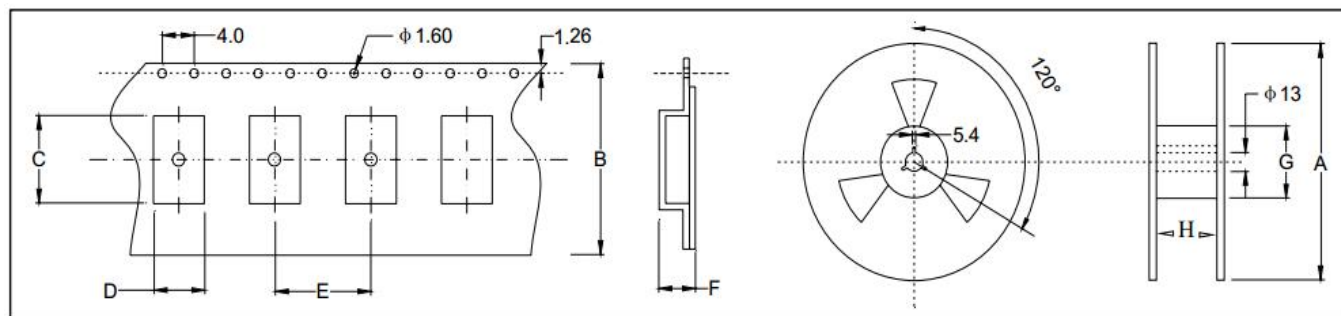
LVDS



LVPECL



Taping Specification(Unit: mm)



Size(OSC)	A	B	C	D	E	F	G	H
SMD-7050	180±2.0	16.0±0.3	7.50±0.1	5.50±0.1	8.0±0.1	2.00±0.1	61.0±1.0	16.0±1.0
SMD-5032	180±2.0	12.0±0.3	5.40±0.1	3.60±0.1	8.0±0.1	1.70±0.1	61.0±1.0	12.0±1.0
SMD-3225	180±2.0	8.0±0.3	3.40±0.1	2.70±0.1	4.0±0.1	1.50±0.1	61.0±1.0	8.0±1.0