SiT5001
1-80 MHz MEMS TCXO and VCTCXO

The Smart Timing Choice™

Features

- Any frequency between 1 and 80 MHz accurate to 6 decimal places
- 100% pin-to-pin drop-in replacement to quartz-based (VC)TCXO
- Frequency stability as low as ±5 ppm. Contact SiTime for tighter stability options
- Ultra low phase jitter: 0.5 ps (12 kHz to 20 MHz)
- Voltage control option with pull range from ±12.5 ppm to ±50 ppm
- LVCMOS compatible output with SoftEdge™ option for EMI reduction
- Voltage control, standby, output enable or no connect modes
- Standard 4-pin packages: 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm
- Outstanding silicon reliability of 2 FIT, 10 times better than quartz
- Pb-free, RoHs and REACH compliant

Applications

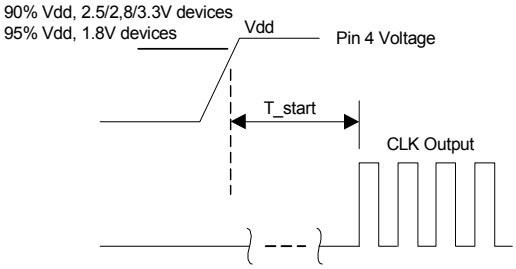
- WiFi, 3G, LTE, SDI, Ethernet, SONET, DSL
- Telecom, networking, smart meter, wireless, test instrumentation

INSTANT SAMPLES | GREEN SOLUTIONS | LIFETIME WARRANTY

Electrical Characteristics

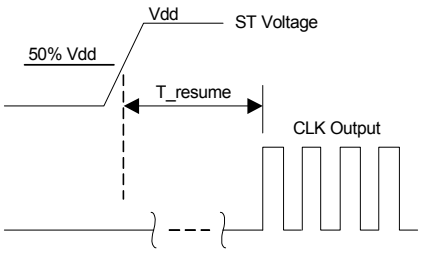
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1	–	80	MHz	
Initial Tolerance	F_init	-1	–	1	ppm	At 25°C after two reflows
Stability Over Temperature	F_stab	-5	–	+5	ppm	Over operating temperature range at rated nominal power supply voltage and load. (*see ordering codes on page 6*) **Contact SiTime for tighter stability options.**
Supply Voltage	F_vdd	–	50	–	ppb	±10% Vdd (±5% for Vdd = 1.8V)
Output Load	F_load	–	0.1	–	ppm	15 pF ±10% of load
First year Aging	F_aging	-2.5	–	+2.5	ppm	25°C
10-year Aging		-4.0	–	+4.0	ppm	25°C
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	Contact SiTime for any other supply voltage options.
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.70	3.0	3.3	V	
		2.97	3.3	3.63	V	
Pull Range	PR	±12.5, ±25, ±50			ppm	
Upper Control Voltage	VC_U	Vdd-0.1	–	–	V	All Vdds. Voltage at which maximum deviation is guaranteed.
Control Voltage Range	VC_L	–	–	0.1	V	
Control Voltage Input Impedance	Z_vc	100	–	–	kΩ	
Frequency Change Polarity	–	Positive slope			–	
Control Voltage -3dB Bandwidth	V_BW	–	–	8	kHz	
Current Consumption	Idd	–	31	33	mA	No load condition, f = 20 MHz, Vdd = 2.5V, 2.8V or 3.3V.
		–	29	31	mA	No load condition, f = 20 MHz, Vdd = 1.8V.
OE Disable Current	I_OD	–	–	31	mA	Vdd = 2.5V, 2.8V or 3.3V, OE = GND, output is Weakly Pulled Down
		–	–	30	mA	Vdd = 1.8 V. OE = GND, output is Weakly Pulled Down
Standby Current	I_std	–	–	70	µA	Vdd = 2.5V, 2.8V or 3.3V, $\overline{ST}$ = GND, output is Weakly Pulled Down.
		–	–	10	µA	Vdd = 1.8V. $\overline{ST}$ = GND, output is Weakly Pulled Down.
Duty Cycle	DC	45	–	55	%	All Vdds
LVCMOS Rise/Fall Time	Tr, Tf	–	1.5	2	ns	LVCMOS option. Default rise/fall time, All Vdds, 10% - 90% Vdd.
SoftEdge™ Rise/Fall Time		SoftEdge™ Rise/Fall Time Table			ns	SoftEdge™ option. Frequency and supply voltage dependent.
Output Voltage High	VOH	90%	–	–	Vdd	OH = -7 mA, IOL = 7 mA, (Vdd = 3.3V, 3.0V) IOH = -4 mA, IOL = 4 mA, (Vdd = 2.8V, 2.5V) IOH = -2 mA, IOL = 2 mA, (Vdd = 1.8V)
Output Voltage Low	VOL	–	–	10%	Vdd	
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z_in	–	100	250	kΩ	

Timing Diagram



T_start: Time to start from power-off

(ST/OE Mode)



T_resume: Time to resume from ST

(ST Mode Only)

Phase Noise Plot